

ABSTRACT OF THE DISCLOSURE

A data bus included in a bi-directional bus circuitry is divided into a first bus node and a second bus node by a repeater circuit. The repeater circuit includes a first tristate buffer for amplifying and transmitting data from the first bus node to the second bus node, and a second tristate buffer connected in reverse direction. When the data bus is not used, the first and second tristate buffers are both activated, and the repeater circuit functions as a latch circuit. Therefore, in the bi-directional bus circuitry, even when the data bus is not used, the potential level of the data bus can be prevented from being left unfixed, ensuring stable operation.

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